Docket No.: SON-1582
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Masumitsu Ino et al.

Application No.: 09/424,544 Confirmation No.: 8128

Filed: November 24, 1999 Art Unit: 2629

For: LIQUID CRYSTAL DISPLAY Examiner: J. J. Piziali

REPLY BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Madam:

This is a Reply Brief under 37 C.F.R. §41.41 in response to the Examiner's Answer mailed on April 14, 2009.

All arguments presented within the Appeal Brief of December 2, 2008 are incorporated herein by reference.

Additional arguments are provided hereinbelow.

Among others, the following positions were presented in the Examiner's Answer, each of which will be addressed in turn in this Reply Brief:

ARGUMENT

Rejection under 35 U.S.C. §112

An Amendment After Appeal Under 37 C.F.R. §41.33 has been filed along with this Reply Brief.

Practice and procedures within the U.S. Patent and Trademark Office pursuant to 37 C.F.R. §41.33(b) provides that Amendments filed on or after the date of filing a brief pursuant to §41.37 may be admitted:

> (1) To cancel claims, where such cancellation does not affect the scope of any other pending claim in the proceeding, or
>
> (2) To rewrite dependent claims into independent form.

While not conceding the propriety of the rejections made within the Final Office Action of May 28, 2008 and in order to advance the prosecution of the present application:

- Claims 25-47 have been canceled;
- Claim 48 has been placed into independent form;
- Claims 50-54 have been canceled;
- Claim 55 has been placed into independent form; and
- Claims 56-78 have been canceled.

Claim 48

All arguments presented within the Appeal Brief of December 2, 2008 are incorporated herein by reference.

Claim 48 includes the features of:

a display portion 10 (specification at figure 5), said display portion 10 having a plurality of gate lines 11, a plurality of signal lines 12 and a plurality of pixels 20 (specification at figure 3, page 9, lines 5-17);

a pixel 20 of said plurality of pixels 20 being located at an intersection of a gate line 11 of said plurality of gate lines 11 and a signal line 12 of said plurality of signal lines 12 (specification at figure 3);

a plurality of driver circuits 14, 44 (specification at page 19, lines 5-6), said plurality of driver circuits 14, 44 including at least one general driver circuit and one remainder driver circuit (specification at figure 5);

each said at least one general driver circuit 14, 44 having a general driver horizontal shift register circuit 31 (specification at figure 4, page 11, line 26 to page 12, line 1) and a plurality of general driver circuit output terminals, a general driver circuit output terminal of said plurality of general driver circuit output terminals providing a signal potential to one of said plurality of signal lines (specification at page 19, lines 5-6);

said remainder driver circuit having a remainder driver horizontal shift register circuit 31 (specification at figure 4, page 11, line 26 to page 12, line 1) and a plurality of remainder driver circuit output terminals, a remainder driver circuit output terminal of said plurality of remainder driver circuit output terminals providing another signal potential to another of said plurality of signal lines (specification at figure 5);

the quantity of remainder driver circuit output terminals being defined as (S – (OP * (DC-1))) (specification at figure 5, page 13, lines 18-21), "S" being the quantity of said plurality of signal lines 12 (specification at page 13, lines 10-13), "OP" being the quantity of general driver circuit output terminals, and "DC" being the quantity of said plurality of driver circuits 14 (specification at figure 5, page 13, lines 21-26);

said quantity of general driver circuit output terminals being different than said quantity of remainder driver circuit output terminals (specification at figure 5),

wherein said plurality of driver circuits 14, 44 are driver integrated circuits arranged in an outside of a transparent insulating substrate on which said display portion 10 is formed.

The specification as originally filed in the paragraph beginning at page 19, line 16, provides the following:

A *plurality of driver ICs* (only a driver IC 44 at the first stage is shown in Fig. 7) to apply a predetermined voltage according to pixel data to the signal lines 42-1, 42-2, 42-3, ... *are provided as external circuits of the liquid crystal display panel 40*. Digital image data which enables a display of, for example, 8 or more gradations and 512 or more colors is inputted to the driver IC 44. The driver IC 44 has a construction shown in, for example, Fig. 4.

Here, the specification as originally filed in the paragraph beginning at page 31, line 19, provides the following:

That is, in the liquid crystal display of the SXGA display system, when the 3-time-divisional driving is used, as shown in Fig. 14, four *driver ICs 44-1 to 44-4* each having 320 output pins are arranged at a predetermined interval *on an external substrate (not shown) different from the liquid crystal display panel 40* and connected to the time-divisional switches (not shown) in the connecting portion 16 of the frame of the liquid crystal display panel 40 through the flexible cables 15.

The specification as originally filed in the paragraph beginning at page 42, line 4, provides the following:

> That is, in case of using the 3-time divisional driving in the liquid crystal display of the UXGA display system, as shown in Fig. 23, five *driver ICs 44-1 to 44-5* each having 320 output pins are arranged at a predetermined interval *on an external substrate (not shown) different from the liquid crystal display panel 40* and connected to the time-divisional switches (not shown) in the connecting portions 16 of the frame of the liquid crystal panel 40 through the flexible cables 15.

Claim 2 as originally filed is drawn to a display according to claim 1, characterized in that said plurality of driver circuits are driver ICs arranged in *an outside of a transparent insulating substrate on which said display portion is formed.*

Claim 6 as originally filed is drawn to a display according to claim 3, characterized in that said plurality of driver circuits are driver ICs arranged in *an outside of a transparent insulating substrate on which said display portion is formed.*

U.S. Patent No. 4,825,203 (Takeda) - Page 7 of the Examiner's Answer asserts the following:

> Furthermore, the examiner takes official notice that one having ordinary skill in the art at the time of invention would recognize that Takeda's shift register circuit [Fig. 1(A): 31] is conventionally comprised by a series of distinct flip-flops set up in a linear fashion which have their inputs and outputs connected together in such a way that the data [Fig. 1(A): D] are shifted down the line [Fig. 1(A): from q_1 to q_N] when the circuit is activated [Fig. 1(A): via clock signal Φ].

In response, there is no concession as to the veracity of any Official Notice taken in the Examiner's Answer.

Instead, U.S. patent practice and procedures dictate that an affidavit or document should be provided in support of any Official Notice taken. 37 C.F.R. §1.104(d)(2), M.P.E.P. § 2144.03.

Here, the use of Official Notice made within the Examiner's Answer is challenged within this Reply Brief.

Specifically, an affidavit or document from the Examiner supporting the use of Official Notice within the Examiner's Answer is respectfully requested.

Note that failure to provide any objective evidence to support the challenged use of Official Notice constitutes ***clear and reversible error***. Ex parte Natale, 11 USPQ2d 1222, 1227-1228 (Bd. Pat. App. & Int. 1989).

Within claim 48, the quantity of remainder driver circuit output terminals being defined as (S – (OP * (DC-1))) (specification at figure 5, page 13, lines 18-21),

> "S" being the quantity of said plurality of signal lines 12 (specification at page 13, lines 10-13),
>
> "OP" being the quantity of general driver circuit output terminals, and
>
> "DC" being the quantity of said plurality of driver circuits 14 (specification at figure 5, page 13, lines 21-26).

Page 6 of the Examiner's Answer contends that Takeda discloses "S" as a value of 5.

In response, there is ***no express teaching*** within Takeda of "S" having a value of 5.

Page 6 of the Examiner's Answer contends that Takeda discloses "OP" as a value of 3.

In response, there is ***no express teaching*** within Takeda of "OP" having a value of 3.

Page 6 of the Examiner's Answer contends that Takeda discloses "DC" as a value of 2.

In response, there is ***no express teaching*** within Takeda of "DC" having a value of 2.

At best, Takeda merely discloses the presence of "N" buffer amps (36) (Takeda at Figure 1), and "j+4" columns (Takeda at Figure 5, column 6, line 42).

No specific amounts are set forth within Takeda.

Thus, Takeda fails to disclose, teach, or suggest the quantity of said remainder driver circuit output terminals being defined as (S – (OP * (DC-1))), "S" being the quantity of said plurality of signal lines, "OP" being the quantity of said general driver circuit output terminals, and "DC" being the quantity of said plurality of driver circuits.

Furthermore, Takeda fails to disclose, teach, or suggest that the quantity of general driver circuit output terminals are different than the quantity of remainder driver circuit output terminals.

Page 14 of the Examiner's Answer asserts the following:

> Regarding claim 48, Takeda discloses said plurality of driver circuits are driver integrated circuits arranged in an outside of a transparent insulating substrate on which said display portion is formed (Fig. 2; Column 2, Line 56 - Column 4, Line 6).

In response, broad conclusory statements, standing alone, are not evidence. *In re Dembiczak*, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999).

Instead, assertions of technical facts in areas of esoteric technology ***must always be supported by citation to some reference work*** recognized as standard in the pertinent art. *In re Pardo and Landau*, 214 USPQ 673, 677 (CCPA 1982). The support must have existed at the time the claimed invention was made. *In re Merck & Co., Inc.*, 231 USPQ 375, 379 (Fed. Cir. 1986).

Here, the assertion set forth within the Examiner's Answer has been presented ***in the absence*** of any objective evidence.

Specifically, Takeda arguably discloses that ***numeral (11)*** in the figure is the ***liquid crystal color display panel*** (Takeda at Figure 2, column 2, lines 58-59).

Switching transistors 11-d are built into the display picture elements 11-c, which are the intersecting points of the row electrodes 11-a and column electrodes 11-b ***on one of the circuit boards of the panel (11)*** (Takeda at column 2, lines 60-64).

On the ***other circuit board***, there are counter electrodes, and respective color filters: red (R), green (G) and blue (B) opposing the display picture elements, arranged, for example, as shown in the diagram (Takeda at column 2, lines 64-67).

Switching elements, for example, thin film transistors or MOS transistors, are provided on the inner surface of *one of the* ***circuit boards*** *that the liquid crystal color display panel is composed of*, picture elements to obtain a display pattern are connected to the respective switching elements, and the electrodes are arranged in a matrix (Takeda at column 3, lines 33-39).

The ***other circuit board*** of the liquid crystal color display panel is provided with counter electrodes opposing the above picture element electrodes and three base color filters: red, green and blue which correspond to the respective picture element electrodes (Takeda at column 3, lines 44-49).

One color filter for each of the picture element electrodes is provided in between the ***two circuit boards*** opposing the respective picture element, and there is an electric field type liquid crystal layer provided in between them which has the same function as a twisted nematic liquid crystal layer (Takeda at column 3, lines 49-54).

Numeral (13) is the ***column electrode drive circuit*** which applies the display signal that includes the color signal to the column electrode line, synchronized with the scanning pulse applied to the row electrode line (Takeda at Figure 2, column 3, lines 4-7).

Nevertheless, the column electrode drive circuit (13) being ***outside of a circuit board*** *on which the liquid crystal color display panel (11) is formed* ***is not disclosed*** within Takeda.

Thus, Takeda fails to disclose, teach, or suggest a display wherein said plurality of driver circuits are driver integrated circuits arranged in an outside of a transparent insulating substrate on which said display portion is formed.

Furthermore, Takeda fails to disclose, teach, or suggest the quantity of general driver circuit output terminals are different than the quantity of remainder driver circuit output terminals.

U.S. Patent No. 5,440,304 (Hirai) - Within claim 48, the quantity of general driver circuit output terminals are ***different*** than the quantity of remainder driver circuit output terminals.

In response, method B requires the circuit configuration as shown in Figure 5, for example (Hirai at column 2, lines 6-7). Figure 5 of Hirai is provided hereinbelow.

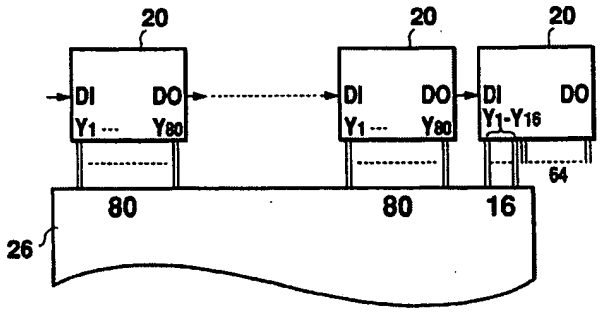


FIG. 5
(PRIOR ART)

However, as shown within Figure 5, ***each*** of the ICs 20 has the ***same number of output terminals***, 80 output terminals in this instance (Hirai at Figure 3).

As a consequence, Hirai ***fails*** to teach the quantity of output terminals for the general driver circuit ICs 20 being ***different*** than the quantity of output terminals for remainder driver circuit IC 20.

Within Hirai, each of the general and remainder driver circuits IC 20 is a device having 80 output terminals (Hirai at Figure 3).

Thus, Hirai fails to disclose, teach, or suggest that the quantity of general driver circuit output terminals are different than the quantity of remainder driver circuit output terminals.

Page 54 of the Examiner's Answer contends that Hirai also, discloses said plurality of driver circuits are driver integrated circuits arranged in an outside of a transparent insulating substrate on which said display portion is formed (Fig. 5; Column 1, Line 5 - Column 2, Line 60).

In response, Hirai arguably discloses that ***the IC 18*** includes a shift register 11, a latch unit 22, a level shifter 23, a driver unit 24, and a shift stage count selection unit 17. The IC 18 includes pins of SELECT 1-SELECT N in addition to DI, DO, CL1, CL2, M, Y_1 -Y_{80}, V, V_{CC}, GND, and V_{EE} (Hirai at column 4, lines 25-30).

To use a cascade of devices of the IC 18 having the configuration shown in FIG. 2 for driving a liquid crystal device 26 of 24 × 24=576 dots, first, eight ICs 18 are connected to ***the liquid crystal device 26*** as shown in FIG. 4 Hirai at column 4, lines 63-67).

Nevertheless, the IC 18 being ***outside of a substrate*** *on which the liquid crystal device 26 is formed* ***is not disclosed*** within Hirai.

Thus, Hirai fails to disclose, teach, or suggest a display wherein said plurality of driver circuits are driver integrated circuits arranged in an outside of a transparent insulating substrate on which said display portion is formed.

Lack of inherency - The feature of the plurality of driver circuits being driver integrated circuits being arranged in an outside of the substrate on which the display portion is formed is a feature that is ***not inherent*** within either Takeda or Hirai.

The Courts have not upheld arguments based on 'inherent' properties when there is no supporting teaching in the prior art" (emphasis added). *In re Dillon*, 13 USPQ2d 1337, 1348 (Fed. Cir. 1989).

The fact that a certain result or characteristic may occur or be present in the prior art ***is not sufficient*** to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993).

Instead, inherency requires that the missing descriptive material is "*necessarily present*," not merely probably or possibly present, in the prior art." *Trintec Indus., Inc. v. Top-U.S.A. Corp.*, 295 F.3d 1292, 1295, 63 USPQ2d 1597, 1599 (Fed. Cir. 2002).

The mere fact that a certain thing *may result* from a given set of circumstances *is* ***not sufficient*** *to show an inherent anticipation. Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1268, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991).

Additionally, such a retrospective view of any alleged "inherent" feature ***is not a substitute*** *for some teaching or suggestion supporting an obviousness rejection. In re Rijckaert,* 28 USPQ2d 195 5, 1957 (Fed. Cir. 1993).

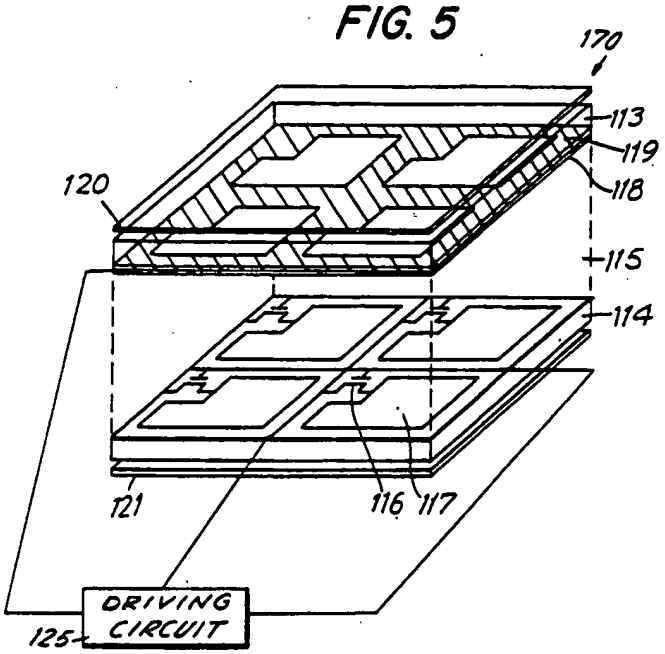
A patentable invention, within the ambit of 35 U.S.C. §103 **may result** even if the inventor has, in effect, merely combined features, old in the art, for their known purpose, without producing anything beyond the results inherent in their use. *In re Sponnoble*, 160 USPQ 237, 243 (CCPA 1969).

For example, U.S. Patent No. 5,191,450 (Yajima) was listed by the Examiner on PTO form 892 in the Office Action of November 13, 2006.

Yajima arguably discloses that light valve 170 is an *active matrix* type liquid crystal valve and includes *a fused quartz lower* ***transparent substrate 114*** (Yajima at column 6, lines 26-28).

Figure 5 of Yajima is provided hereinbelow.

FIG. 5



However, a ***driving circuit 125*** shown in FIGS. 12(a), 12(b), 12(c) and 12(d) may be ***formed on the interior surface of substrate 114*** (Yajima at column 6, lines 28-30).

Taking Yajima into consideration, the column electrode drive circuit (13) of Takeda being *outside of a circuit board* on which the liquid crystal color display panel (11) is formed ***is not necessarily present*** within Takeda.

Taking Yajima into consideration, the IC 18 of Hirai being *outside of a substrate* on which the liquid crystal device 26 is formed ***is not necessarily present*** within Hirai.

Thus, the feature of the plurality of driver circuits being driver integrated circuits being arranged in an outside of the substrate on which the display portion is formed is a feature that is not inherent within either Takeda or Hirai.

Claim 55

All arguments presented within the Appeal Brief of December 2, 2008 are incorporated herein by reference.

Claim 55 is drawn to a display having:

a display portion 10 (specification at Figure 6), said display portion 10 having a plurality of gate lines 11, a plurality of signal lines 12 and a plurality of pixels 20 (specification at figure 3, page 9, lines 5-17);

a pixel 20 of said plurality of pixels 20 being located at an intersection of a gate line 11 of said plurality of gate lines 11 and a signal line 12 of said plurality of signal lines 12 (specification at figure 3);

a plurality of driver circuits 14, 44, each of said plurality of driver circuits 14, 44 having a plurality of driver circuit output terminals;

a driver circuit output terminal of said a plurality of driver circuit output terminals providing a signal potential to a signal line of said plurality of signal lines (specification at page 19, lines 5-6);

the quantity of said driver circuit output terminals being the same quantity for said each of said plurality of driver circuits 14, 44 (specification at figure 6);

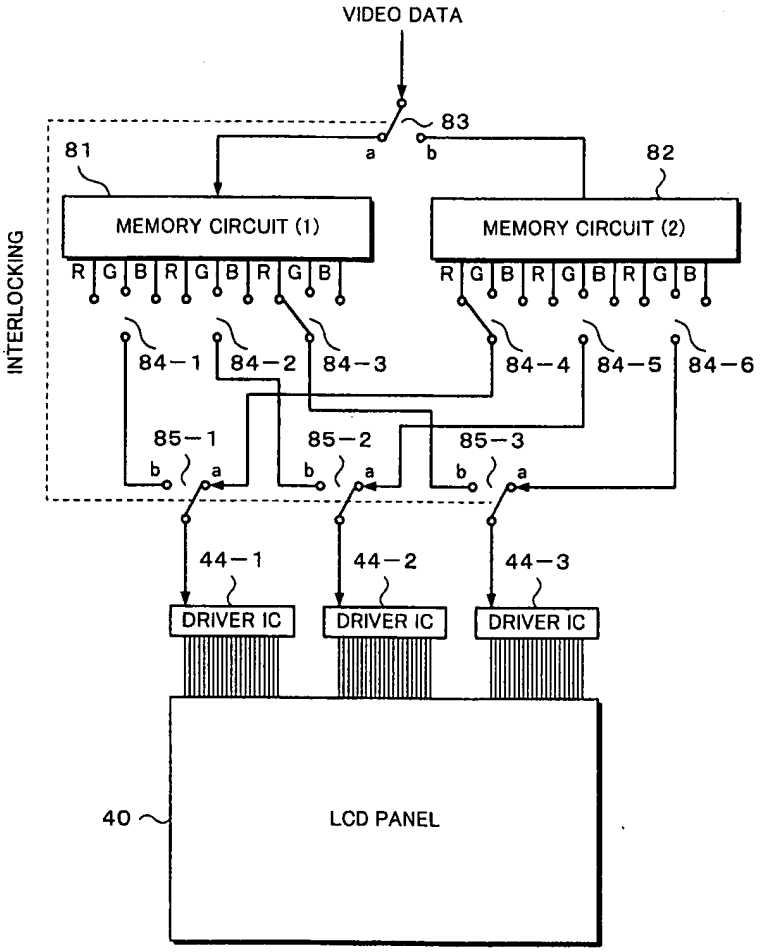
the quantity of said driver circuits 14, 44 being defined as N/n, wherein "N" is the quantity of said signal lines and "n" is said quantity of said driver circuit output terminals (specification at page 44, lines 23-26);

a memory circuit 81, 82 for temporarily storing data to be written into said plurality of driver circuits 14, 44; and

a control circuit for controlling said plurality of driver circuits 14, 44 so as to simultaneously write different data from said memory circuit 81, 82 (specification at figure 31, page 47, line 23 to page 50, line 18).

Figure 31 of the specification as originally filed is provided hereinbelow.

Fig. 31



The specification as originally filed at page 48, line 27, to page 49, line 3, provides that *when one of the switches 83 and the switches 85-1 to 85-3 selects the memory circuit 81, the other selects the memory circuit 82.*

Takeda - Within claim 55, the quantity of said driver circuits being defined as N/n, wherein "N" is the quantity of said signal lines and "n" is said quantity of said driver circuit output terminals.

Page 21 of the Examiner's Answer "arbitrarily sets N =6 column signal lines".

In response, there is ***no express teaching*** within Takeda of only 6 column signal lines.

Page 22 of the Examiner's Answer asserts the presence of only 2 driver circuit output terminals.

In response, there is ***no express teaching*** within Takeda of only 2 driver circuit output terminals.

Thus, Takeda fails to disclose, teach, or suggest the quantity of said driver circuits being defined as N/n, wherein "N" is the quantity of said signal lines and "n" is said quantity of said driver circuit output terminals.

Figures 1(A) and 2 of Takeda are provided hereinbelow.

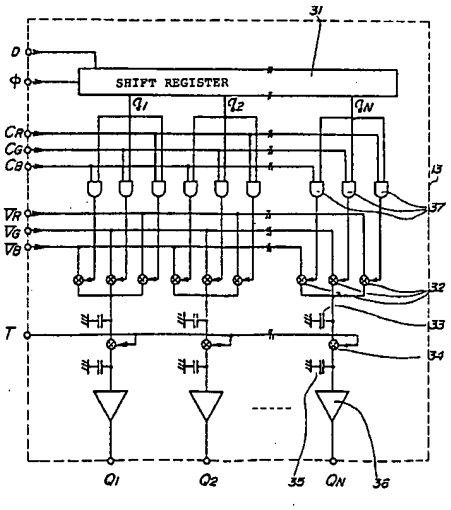
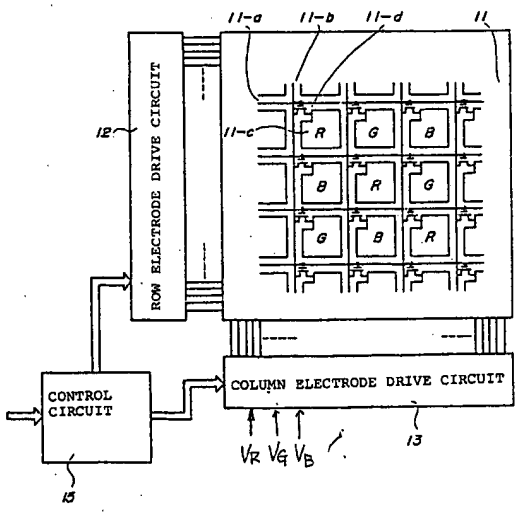


FIG. 1(A)

FIG. 2



Page 20 of the Examiner's Answer identifies element 13 of Takeda as a column electrode drive circuit.

In this regard, no circuitry within Takeda that has been identified within the Examiner's Answer that is capable of storing data, then writing that data into the alleged column electrode drive circuit 13.

For example, page 24 of the Examiner's Answer identifies element 31 of Takeda as the alleged memory circuit.

However, page 20 of the Examiner's Answer identifies element 31 of Takeda as being part of the alleged column electrode drive circuit 13.

By analogy, Examiner's Answer identifies *the alleged memory circuit 31 of Takeda **as being part** of the alleged column electrode drive circuit 13*.

However, Takeda ***fails*** to disclose the alleged memory circuit 31 of Takeda as being capable of storing data, then writing that data into the alleged column electrode drive circuit 13 since the alleged memory circuit 31 of Takeda has been indicated within the Examiner's Answer as being part of the alleged column electrode drive circuit 13.

Stated succinctly, data that has been written into the alleged memory circuit 31 of Takeda ***has already been written*** into the alleged column electrode drive circuit 13 since the alleged memory circuit 31 has been identified as ***being a part of*** the alleged column electrode drive circuit 13.

As a consequence, the Examiner's Answer has ***failed*** to identify any circuitry within Takeda that is capable of storing data ***prior to*** that data being written into the alleged column electrode drive circuit 13.

Thus, Takeda fails to disclose, teach, or suggest a memory circuit for temporarily storing data to be written into said plurality of driver circuits.

Page 24 of the Examiner's Answer contends that Takeda discloses the presence of control circuit 15.

In response, Takeda arguably discloses that numeral (15) is the control circuit which controls the operation of the above circuits (Takeda at column 3, lines 8-9).

However, Takeda ***fails*** to disclose, teach, or suggest the control circuit 15 as controlling the alleged driver circuits of Takeda so as to simultaneously write different data from the alleged memory circuit 31 of Takeda.

Thus, Takeda fails to disclose, teach, or suggest a control circuit for controlling said plurality of driver circuits so as to simultaneously write different data from said memory circuit.

Hirai - The Examiner's Answer has ***failed*** to identify any circuitry within Hirai that is capable of storing data ***prior to*** that data being written into the alleged column electrode drive circuit.

Thus, Hirai fails to disclose, teach, or suggest a memory circuit for temporarily storing data to be written into said plurality of driver circuits.

Moreover, Hirai fails to disclose, teach, or suggest a control circuit for controlling said plurality of driver circuits so as to simultaneously write different data from said memory circuit.

Lee - The Examiner's Answer has ***failed*** to identify any circuitry within Lee that is capable of storing data ***prior to*** that data being written into the alleged column electrode drive circuit.

Thus, Lee fails to disclose, teach, or suggest a memory circuit for temporarily storing data to be written into said plurality of driver circuits.

Moreover, Lee fails to disclose, teach, or suggest a control circuit for controlling said plurality of driver circuits so as to simultaneously write different data from said memory circuit.

U.S. Patent No. 4,745,406 (Hayashi) - The Examiner's Answer has ***failed*** to identify any circuitry within Hayashi that is capable of storing data ***prior to*** that data being written into the alleged column electrode drive circuit.

Thus, Hayashi fails to disclose, teach, or suggest a memory circuit for temporarily storing data to be written into said plurality of driver circuits.

Moreover, Hayashi fails to disclose, teach, or suggest a control circuit for controlling said plurality of driver circuits so as to simultaneously write different data from said memory circuit.

CONCLUSION

The prior art of record fails to disclose, teach or suggest all the features of the claimed invention. For the foregoing reasons, all the claims now pending in the present application are allowable, and the present application is in condition for allowance. For at least the reasons set forth hereinabove, the rejection of the claimed invention should not be sustained.

Therefore, a reversal of the rejection of May 28, 2008 is respectfully requested.

If any additional fee is required or any overpayment made, the Commissioner is hereby authorized to charge the fee or credit the overpayment to Deposit Account # 18-0013.

Dated: June 15, 2009

Respectfully submitted,

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EVIDENCE APPENDIX

U.S. Patent No. 5,191,450 (Yajima) listed by the Examiner on PTO form 892 in the Office Action of November 13, 2006.

There is no other evidence which will directly affect or have a bearing on the Board's decision in this appeal.